



**Programmable
Serial
Interface
Adapter**

**Model
PSIA-2722**

The Audio Precision Programmable Serial Interface Adapter (PSIA) facilitates the connection of chip-level devices, such as analog-to-digital converters, digital-to-analog converters and sample-rate converters to a System Two Cascade or Cascade Plus measurement instrument. Devices may have a variety of interface protocols: different logic families and voltage levels, clock rates, word orientations, and formats.

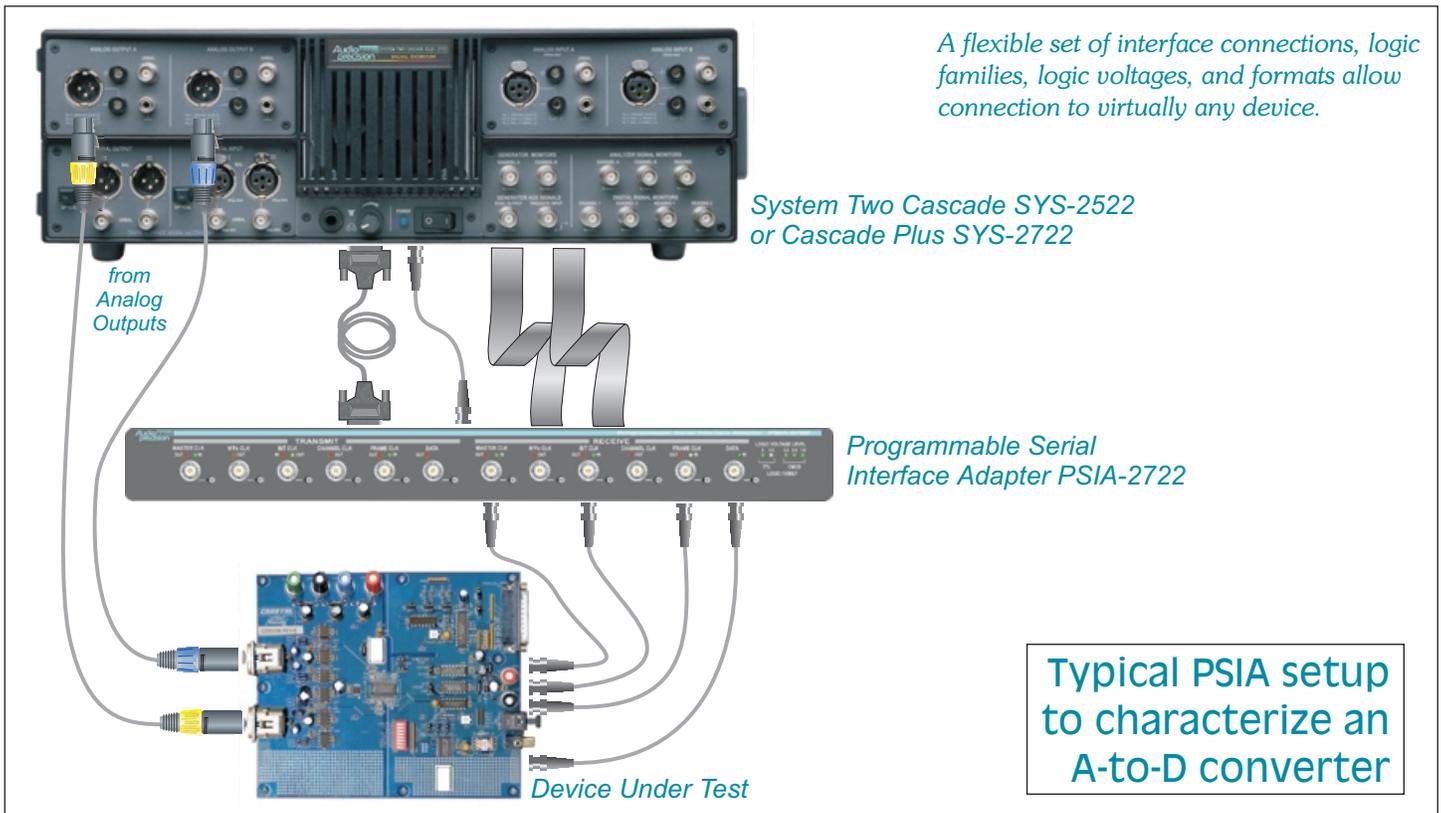
User interface

The PSIA accommodates a wide variety of parameters to allow connection to virtually any device. These parameters

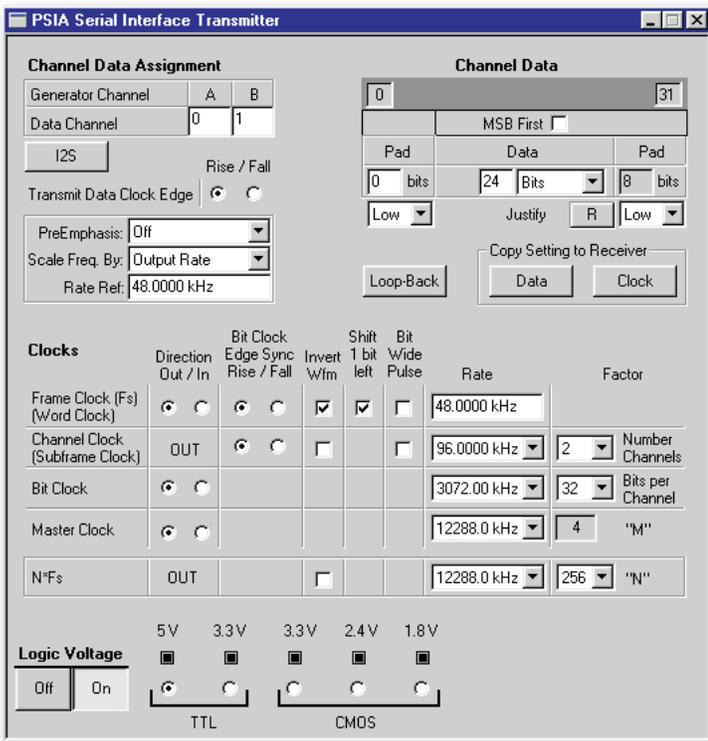
are set within the Cascade or Cascade Plus control software, APWIN, on easy-to-use soft Transmitter and Receiver panels. PSIA setups are saved as part of the Cascade or Cascade Plus test file, ensuring repeatable and consistent measurements.

Accommodates new logic families

The PSIA can accommodate the latest low-level logic, offering voltage levels and sensitivity selectable for CMOS devices at 1.8 V, 2.4 V and 3.3 V, or TTL devices at 3.3 V and 5 V.



**Typical PSIA setup
to characterize an
A-to-D converter**



All device parameters are set using soft panels like the one illustrated here. Clock rates, word width and format, data channels and other parameters can be set and saved to allow easy and predictable device tests. Panels are included for transmit and receive functions with the ability to copy settings from one to the other.

The panel shown is the Transmitter panel; the separate Receiver panel is similar.

Comprehensive Clock Capabilities

The PSIA-2722 offers independent control of the word and bit clock with either an internal or external source. A channel (subframe) clock is provided as well as a selectable clock multiplier output (N*Fs). Settings are included for inversion, bit-wide pulse, and edge sync. The intuitive soft control panel allows clock settings to be set by rate or factor.

- I²S switch
- Internal or external master clock, bit clock, and word clock
- Channel (subframe) clock output
- N*Fs clock output
- Settings for inversion, bit-wide pulse, and edge sync
- Intuitive clock settings by rate or factor

Operates with Variety of Logic Families

Controls are included to select any of four voltage levels and either TTL or CMOS logic family. The data format and bit orientation can be selected from a wide set of choices to match device requirements. 2, 4 or multiple channels are supported.

- Voltage levels for 5 V to 1.8 V with front panel LED logic voltage indicators
- Variable data word width
- MSB or LSB first
- Left justified, right justified, or padded
- Data padding with "0", "1", or sign/LSB

Convenient Test Development Features

The PSIA includes a Loop-Back mode to facilitate debugging. You can copy transmitter settings to the receiver with a single click for quick setup. The complete setup can be stored and recalled with APWIN tests. Simplified setup controls for I²S are also provided.

Package

The PSIA is housed in a slim rack-width package that will conveniently sit on top of the host Cascade Plus system. All logic lines are connected via front panel BNC connectors to ensure data integrity. A handy oscilloscope probe jack is provided for each BNC signal. As several of the data ports can be either in an input or output mode, LEDs are located above each BNC connector to indicate data direction.



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